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Attorney's Docket No.: 030681-576

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Joon-seop Kwak et al.	Group Art Unit: 2812
Application No.: 10/673,251	Examiner: SAVITRI MULPURI
Filed: September 30, 2003	Appeal No.: _____
For: GaN Based Group ii-V Nitride Semiconductor Light-Emitting Diode and Method for Fabricating the Same	

APPEAL BRIEF

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal is from the decision of the Primary Examiner dated September 3, 2004 (Paper No. 20040901), finally rejecting claims 1-4, 6, 9-27 and 31-35, which are reproduced as the Claims Appendix of this brief.

☒ A check covering the ☐ $250.00 (2402) ☒ $500.00 (1402) Government fee is filed herewith.

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The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800.

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I. Real Party in Interest

The present application is assigned to Samsung Electro-mechanics Co., Ltd.

II. Related Appeals and Interferences

The Appellants' legal representative, and assignee do not know of any other appeal or interferences which may be related to, directly affect, or be directly affected by or have bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-4, 6, 9-27 and 31-35 are currently pending, stand finally rejected by the Examiner and are appealed. Claims 5, 7, 8, 28, 29 and 30 have been canceled.

IV. Status of Amendments

No amendments have been filed subsequent to the final Office Action.

V. Summary of Claimed Subject Matter

The claim sets are divided into two categories. Claims 1-4, 6, 9-22 are supported by the light emitting diode (LED) embodiments shown in Figures 5-8. This grouping of claims is further divided into two sets. Claim 1 and dependent claims 3, 4, 6 and 9-11 are supported by the LED embodiments of Figures 5 and 7, whereas independent claim 12 and dependent claims 13-22 are supported by the LED embodiments of Figures 6 and 8.

Claims 23-27, 31-35 are supported by the laser diode embodiments of Figures 17-22.

Claim 1

Claim 1 recites a method for fabricating a light-emitting device which includes sequentially forming a first compound semiconductor layer (Figs. 5 and 7, 58), an active layer (56), and a second compound semiconductor layer (54), which are for inducing light emission, on a high-resistant substrate (60).[1] In Figures 5 and 7, a light-*transmitting* conductive layer (50) is located on the second compound semiconductor layer; meaning that light is emitted from the top surface of the LED as depicted in Figures 5 and 7. The method further includes dry etching a region (Fig. 5, 62; Fig. 7, areas other than 60a) of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first compound semiconductor layer. The last step of independent claim 1 includes forming a light-shielding conductive layer (Figs. 5 and 7, 64 and 80, respectively).

[1] The inclusion of reference numbers in this description is done to facilitate consideration of the claims by showing support therefor in the originally filed specification. The claims are not limited to these specific embodiments.

The embodiments covered by claim 12 are similar in structure but the reflective and light transmitting conductive layers are reversed in orientation. Specifically, in Figures 6 and 8, a light *reflecting* conductive layer 70 is placed on the second compound semiconductor layer as in the embodiment shown in Figure 8. The light transmitting conductive layer (Figure 6, 72; Figure 8, 82) covers the exposed region on the first compound semiconductor layer.

As will be apparent from the discussion in the arguments section, claims 1 and 12 are independently patentable with respect to one another because of the relative location of the light transmitting and light reflecting conductive layers.

With respect to claim 23 and the laser diode embodiments of Figures 9-22 for instance, the present invention is embodied in a method of fabricating a light-emitting device (e.g., a laser diode) which includes forming a material layer (Figs. 9-22, 152, 158, 160, 162) on a high-resistant substrate (150). The method includes forming a first electrode (154) on the material layer. As recited in claim 23, the method includes dry etching a region (Figure 10, age 3; Figure 11, age 4, Figure 12, unmarked; Figures 13-22, horizontal area other than 150) of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose a region of the material layer. Finally, claim 23 recites forming a second electrode (156) on the bottom of the high-resistant substrate to cover partially or fully the exposed region of the material layer.

VI. Grounds of Rejection to be Reviewed on Appeal

The Office Action maintains the rejection of claims 1-4, 6, 9-27 and 31-35 under 35 U.S.C. §103 as allegedly being unpatentable over the *Kawai* patent (U.S. Patent No. 6,468,902) in combination with the *Nunoue* patent (U.S. Patent No. 5,905,275).

VII. Argument

With respect to claims 1 and 23 (and claims dependent therefrom) Appellants respectfully (1) submits that the applied art supplies no reason to combine the references, (2) contest the Examiner's characterization of the applied art, and (3) contend that even assuming *arguendo* the disclosures of the *Kawai* and *Nunoue* patents could be combined in some fashion, the hypothetical result would not meet the recitations of the pending claims.

As appropriately summarized in the MPEP, three criteria must be met to establish a prima facie case of obviousness. First, the cited documents must describe or suggest all of the claim features. Second, there must be some suggestion or motivation, either in the cited documents themselves or in the knowledge generally available to one of ordinary skill in the art, to have combined the teachings of the cited documents. Third, there must have been a reasonable expectation that the documents could have been successfully combined to yield the claimed invention.

No Reason to Combine the Applied Art - "Teaching away"

The obviousness rejection raised in the Action should not stand because, as admitted in the Action, the *Kawai* patent does not describe "dry etching a region of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first compound semiconductor layer". The required motivation to combine the *Kawai* patent with any document, much less the *Nunoue* patent, to prove a prima facie case is lacking.

For example, Kawai states at col. 2, ll. 37-44, that:

> Also regarding the via hole to be made in the sapphire substrate, since sapphire is very stable in chemical property, wet etching cannot be used without any effective etchant. As to dry etching by RIE, since its etching rate is as very low as several μm/hr in maximum, and there is no etching mask having a selectivity acceptable for selective etching. Therefore, it is actually impossible to make the via hole with any of these methods. (emphasis added)

The *Kawai* patent further states at col. 4, ll. 52-53, that "[f]or making the via hole, dry etching such as conventional RIE cannot be employed".

Such strong and unambiguous language would discourage persons skilled in the art at the time of the invention to combine the *Kawai* patent with any document, including the *Nunoue* patent, that advocates dry etching a region of the high-resistant substrate, such as sapphire, as recited in claims 1 and 23.

The Combination Lacks All the Features of the Independent Claims

In addition to strongly discouraging the use of a dry-etch process to form its via hole, the *Kawai* patent describes in detail a wet-etch process in which the bottom surface side of a sapphire substrate 1 is immersed into an etchant of phosphoric/sulfuric acid solution held at approximately 280°C. Although the *Kawai* patent describes that a dry-etch RIE process can be used to etch part of the GaN semiconductor layer 2 exposed at the bottom of the via hole 8 previously removed by the wet-etch process, it is clear from the document that the sapphire substrate 1 is not etched using the dry-etch RIE process. *See*, col. 5, ll. 8-10 and 15-17.

Moreover, the *Kawai* patent describes in conjunction with the embodiment shown in FIG. 14, that "using the same [wet-etch] method as used in the first and second embodiments, the via hole 61 is made by selecting (sic) removing a part of the c-plane sapphire substrate in alignment with the p-side electrode 60 from the bottom thereof." Col. 13, ll. 37-41.

Accordingly, independent claims 1 and 23, are considered allowable over the combination of the *Kawai* and *Nunoue* patents because neither of the documents describe or suggest all of the claimed features, and because the requisite motivation to combine the cited documents is lacking. The claims that depend from claims 1 and 23 are considered to be allowable for at least these same reasons.

The Examiner Mischaracterizes the Applied Art

The *Kawai* patent illustrates a GaN semiconductor laser in Figure 14. It includes a sapphire substrate 51 through which a via hole 61 is formed. An n-side Ti/Al electrode 61 is placed in the via hole 61 to make ohmic contact with the n-type GaN contact layer 53.

A major emphasis of the *Kawai* patent is that the via hole 61 is formed through a wet etch process. See col. 13, lines 36-47 and its implicit reference to col.11, lines 18-36 as well as col. 10, lines 53-60, for instance, explaining the wet etch process.

The *Kawai* patent includes the statement that it is impossible to make a via hole in a sapphire substrate using other methods such as dry etching by RIE (see col. 2, lines 37-44 and col. 4, lines 52-53).

The Examiner acknowledges that the *Kawai* patent does not teach etching the sapphire substrate by a mixture of chlorine and argon but he suggests that the *Nunoue* patent discloses such a method and that its teachings are sufficient to overcome *Kawai's* clearly negative teaching that dry etching a sapphire substrate is not possible.

What the *Nunoue et al.* patent actually discloses, however, is a method of forming a trench by a reactive ion beam etching using Cl_2/Ar gas mixture and thereafter removing the layer damaged by the dry etching using a phosphoric acid etchant to thereby form the trench as illustrated in Figures 1a-1d. Thereafter, a multi-layered structure is formed in the trench. As shown in Figure 1c, the sapphire substrate is polished until the buffer layer is exposed. Hence, in the embodiment shown in Figure 1, the *Nunoue et al.* patent actually discloses a mechanical mechanism for exposing the buffer layer forming part of the stack of layers on the sapphire substrate.

Insofar as the rejection depends on a mischaracterization of the applied art, the rejection cannot stand and should be overturned.

The Hypothetical Combination Does Not Meet the Claim Recitations

Even if one were to accept, *arguendo*, the Examiner's position that the teachings of the *Nunoue et al.* are sufficiently strong to overcome the very explicit negative teaching that RIE dry etching is inappropriate for sapphire substrates in forming via holes, the hypothetical combination of these two teachings would be that the multi-layer structure of Kawai's Figure 14 should be formed in a trench and thereafter the sapphire substrate mechanically polished to expose the bottom most layers of the multi-layer structure.

Such hypothetical combination would not meet the steps of independent method claims 1 and 23 which include dry etching a region of the high resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first compound semiconductor layer. The first compound semiconductor layer of the *Kawai* patent, employing the hypothetical combination of teachings, would be exposed through a polishing step that would actually involve a much different method from what is recited in independent claims 1 and 23.

With respect to the embodiment of Figures 7a-7g of the *Nunoue et al.* patent, it is noted the tapered contact hole 62 is formed in the first sapphire substrate 61 before any functional layers are formed on the first sapphire substrate 61. The contact hole 62 is formed by various mechanical, laser light and chemical processes such as chemical etching by phosphoric acid etchant. Thereafter, there are performed relatively elaborate processes of attaching a second sapphire substrate 64 onto a buffer layer 63 which in turn is formed on the first sapphire substrate 61, forming a barrier layer 65, removing the second sapphire substrate 64 and forming the multiple layers of semiconductor material on the first sapphire substrate 61.

Again, even if one were to assume for a moment that the *Nunoue et al.* patent teachings were sufficiently strong to overcome the clear negative teachings in the *Kawai* patent, the hypothetical result would not be the combination of method steps recited in either independent claims 1 or 23 insofar as the hypothetical combination would still not involve a dry etching step wherein a region of the high resistant substrate is etched using a reaction gas comprising at least Cl_2 or BCl_3 to expose the

first compound semiconductor layer. The hypothetical combination of teachings would result only in a method where the sapphire substrate would have a contact hole formed therein before any compound semiconductor layers are formed thereon and would involve multiple additional steps involving second sapphire substrates, etc. Succinctly, the hypothetical combination would not result in the combination of steps found in independent claims 1 or 23.

It is respectfully submitted that with respect to claims 1-4, 6, 9-11, 23-27, 31-35, even assuming hypothetical combination proposed in the Office Action, the hypothetical result would not meet the recitations of these claims.

Independent Claim 12

With respect to claim 12, it is noted that a light-transmitting conductive layer is recited to cover the exposed region on the first compound semiconductor layer, which had been exposed by etching a region of the high-resistant substrate, as recited in claim 12. The Examiner takes the position that it is "well known in the art to form first and second electrodes, which are made of either light reflective or light transmitting materials (see admitted prior art, para 006 and figure 1)." The *Nunoue et al.* patent appears to be silent with regard to whether either the electrodes are transparent and the *Kawai* patent clearly discloses that the bottom electrode conductive layer 36/37 covering the exposed region of the GaN semiconductor layer 22 consists of chromium and gold. It is respectfully submitted that it would be understood that these materials are not light transmitting as employed in the *Kawai* device.

It is apparent that the applied prior art did not appreciate that light could be transmitted through the substrate via the portion that had been removed to expose the first compound semiconductor layer. The mere fact that both transparent and non-transparent electrodes are used in light emitting semiconductor structures does not suggest using a transparent electrode on a removed portion of a substrate particularly because this electrode is disclosed as being non-transparent.

Claim 12 recites, among other things, "sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate", "etching a region of the high-resistant substrate to expose the first compound semiconductor layer", and "forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer". Accordingly, the first compound semiconductor layer is arranged on the high-resistant substrate, and a light-transmitting conductive layer is formed to cover a region of the first compound semiconductor layer exposed through a corresponding exposed region of the high-resistant substrate. The *Kawai* and *Nunoue et al.* patents do not describe these features.

The first compound semiconductor recited in claim 12 can read only on the exposed regions of Kawai's GaN semiconductor layer 22 shown in FIG. 11 and the GaN buffer/contact layer 52/53 shown in FIG. 14. The *Kawai* patent describes that the conductive layer 36/37 covering the exposed region of GaN semiconductor layer 22 in FIG. 11 consists of chromium (Cr) and gold (Au). As suggested above, persons skilled in the art would understand that these metal layers are not light-transmitting as the claim recites, but instead are light-reflecting layers. The Office admits as much on page 3 of the Action. Likewise, the *Kawai* patent describes that the conductive layer 62 covering the exposed region of the GaN buffer/contact layer 52/53 shown in FIG. 14 consists of titanium (Ti) and aluminum (Al), which are also not light-transmitting layers. The *Nunoue* patent does not supply the necessary teachings to suggest a modification to the *Kawai* device in this regard.

Accordingly, the Applicants respectfully assert that claim 12 is allowable over the combination of the *Kawai* patent at least because the cited documents do not describe forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer. Moreover, dependent claims 13-22 are considerable allowable for at least this same reason.

VIII. Claims Appendix

See attached Claims Appendix for a copy of the claims involved in the appeal.

IX. Evidence Appendix

Attached Evidence Appendix includes no copies of evidence as none was relied upon by Appellant.

X. Related Proceedings Appendix

Attached Related Proceedings Appendix includes no copies of decisions as none were identified in Section II, supra.

XI. Conclusion

In light of the foregoing, Appellants respectfully request that the Examiner's rejection be overturned.

Respectfully submitted,

Burns, Doane, Swecker & Mathis, L.L.P.

Date June 2, 2005

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VIII. CLAIMS APPENDIX

The Appealed Claims

Claim 1: A method for fabricating a light-emitting device, the method comprising:

(a) sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate;

(b) forming a light-transmitting conductive layer on the second compound semiconductor layer;

(c) dry etching a region of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first compound semiconductor layer; and

(d) forming a light-shielding conductive layer to cover the exposed region of the first compound semiconductor layer.

Claim 2: The method of claim 1, wherein step (c) comprises:

polishing the bottom of the high-substrate; and

exposing the bottom of the first compound semiconductor layer by etching the region of the high-resistant substrate.

Claim 3: The method of claim 2, wherein the high-resistant substrate is a sapphire substrate.

Claim 4: The method of claim 2, wherein the bottom of the high-resistant substrate is polished by grinding or lapping.

Claim 5 (canceled).

Claim 6: The method of claim 1, wherein the reactant gas further comprises Ar gas.

Claim 7-8 (canceled).

Claim 9: The method of claim 2, wherein the high-resistant substrate is etched to form a via hole through which the bottom of the first compound semiconductor layer is exposed.

Claim 10: The method of claim 2, wherein the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching.

Claim 11: The method of claim 1, further comprising forming a pad layer on the light-transmitting conductive layer.

Claim 12: A method for fabricating a light-emitting device, the method comprising:

(a) sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate;

(b) forming a light-reflecting conductive layer on the second compound semiconductor layer;

(c) etching a region of the high-resistant substrate to expose the first compound semiconductor layer; and

(d) forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer.

Claim 13: The method of claim 12, wherein step (c) comprises:

polishing the bottom of the high-resistant substrate; and

exposing the bottom of the first compound semiconductor layer by etching the region of the high-resistant substrate.

Claim 14: The method of claim 13, wherein the high-resistant substrate is a sapphire substrate.

Claim 15: The method of claim 13, wherein the bottom of the high-resistant substrate is polished by grinding or lapping.

Claim 16: The method of claim 12, wherein the high-resistant substrate is dry etched using a reaction gas comprising at least Cl_2 or BCl_3.

Claim 17: The method of claim 16, wherein the reactant gas further comprises Ar gas.

Claim 18: The method of claim 13, wherein the high-resistant substrate is dry etched using a reaction gas comprising at least Cl_2 or BCl_3.

Claim 19: The method of claim 18, wherein the reactant gas further comprises Ar gas.

Claim 20: The method of claim 13, wherein the high-resistant substrate is etched to form a via hole through which the bottom of the first compound semiconductor layer is exposed.

Claim 21: The method of claim 13, wherein the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching.

Claim 22: The method of claim 12, further comprising forming a pad layer on the light-transmitting conductive layer.

Claim 23: A method for fabricating a light-emitting device, the method comprising:

(a) forming a material layer for lasing on a high-resistant substrate;

(b) forming a first electrode on the material layer;

(c) dry etching a region of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose a region of the material layer; and

(d) forming a second electrode on the bottom of the high-resistant substrate to cover partially or fully the exposed region of the material layer.

Claim 24: The method of claim 23, wherein step (a) comprises:

sequentially forming a first compound semiconductor layer, a first cladding layer, a resonator layer, a second cladding layer, and a second compound semiconductor layer on the high-resistant substrate;

forming a mask pattern on the second compound semiconductor layer to cover a predetermined region of the second compound semiconductor layer;

sequentially patterning the second compound semiconductor layer and the second cladding layer using the mask pattern as an etch mask, the second cladding layer into a rigid form;

removing the mask pattern; and

forming a passivation layer on the second cladding layer patterned into the ridge form, in contact with a region of the patterned second compound semiconductor layer.

Claim 25: The method of claim 24, wherein step (c) comprises:

polishing the bottom of the high-resistant substrate; and

exposing the bottom of the first compound semiconductor layer by etching the region of the high-resistant substrate.

Claim 26: The method of claim 25, wherein the high-resistant substrate is a sapphire substrate.

Claim 27: The method of claim 25, wherein the bottom of the high-resistant substrate is polished by grinding or lapping.

Claim 28-30 (canceled).

Claim 31: The method of claim 24, wherein the reactant gas further comprises Ar gas.

Claim 32: The method of claim 25, wherein the high-resistant substrate is etched to form a via hole through which the bottom of the first compound semiconductor layer is exposed.

Claim 33: The method of claim 25, wherein the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching.

Claim 34: The method of claim 24, wherein the resonator layer is formed by sequentially forming a first waveguide layer, an active layer, and a second waveguide layer on the first cladding layer.

Claim 35: The method of claim 23, wherein step (d) comprises:

forming an ohmic contact layer on the bottom of the high-resistant substrate to cover partially or fully the exposed region of the material layer; and

forming a thermal conductive layer on the ohmic contact layer.

IX. EVIDENCE APPENDIX

N/A

X. RELATED PROCEEDINGS APPENDIX

N/A